Curriculum Framework – Digital Electronics – (2015-2016)
Unit 2 Combinational Logic – Lesson 2.2 Alternative Design: Universal Gates and K-Mapping

Desired Results *(stage 1)*

ESTABLISHED GOALS
It is expected that students will…

- G1 – Demonstrate an ability to identify, formulate, and solve engineering problems.
- G2 – Demonstrate an ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability.
- G3 – Demonstrate an ability to design and conduct experiments, as well as to analyze and interpret data.
- G4 – Demonstrate an ability to apply knowledge

Transfer

TRANSFER: *Students will be able to independently use their learning to …*

- T1 – Recognize and apply alternative design strategies to AOI logic design. (Universal Gates)
- T2 – Recognize and apply alternative simplification strategies to Boolean algebra. (K-Mapping)
- T3 – Evaluate and determine when alternative design strategies are beneficial to a circuit's design or design process.

Meaning

UNDERSTANDINGS: *Students will understand that …*

- U1 – There is a formal design process for translating a set of design specifications into a functional combinational logic circuit implemented with NAND or NOR gates.
- U2 – Combinational logic designs implemented with NAND gates or NOR gates will typically require fewer Integrated Circuits (IC) than AOI equivalent implementations.
- U3 – A NAND gate is considered a universal gate because it can be used to implement an AND gate, OR gate, and an INVERTER gate. Any combinational logic expression can be implemented using only NAND gates.
- U4 – A NOR gate is considered a universal gate because it can be used to implement an AND gate, OR gate, and an INVERTER gate. Any

ESSENTIAL QUESTIONS: *Students will keep considering …*

- Q1 – Why are NAND gates and NOR gates considered universal gates?
- Q2 – What are the advantages of implementing a combinational logic design with universal gates?
- Q3 – What are the advantages of using K-mapping over Boolean algebra to simplify logic expressions?

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of mathematics, science, and engineering. • G5 – Demonstrate an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice. • G6 – Pursue the broad education necessary to understand the impact of engineering solutions in a global, economic, environmental, and societal context. • G7 – Demonstrate an understanding of professional and ethical responsibility. • G8 – Demonstrate an ability to function on multidisciplinary teams. • G9 – Demonstrate an ability to communicate effectively. • G10 – Gain knowledge of contemporary issues. • G11 – Recognize the need for, and develop an ability to engage in life-long learning.	combinational logic expression can be implemented using only NOR gates. • U5 – Karnaugh Mapping is a graphical technique for simplifying logic expressions containing two, three, and four variables. • U6 – A don't care condition is a situations where the design specifications "don't care" what the output is for one or more input conditions. Don't care conditions in K-Maps can lead to significantly simpler logic expressions and circuit implementations.	
	Acquisition	
	KNOWLEDGE: *Students will…* • K1 – Identify NAND and NOR gates and recognize them as universal gates. U3,U4 • K2 – Know that universal gates may provide the opportunity for a more efficient design. U1,U2 • K3 – Relate AOI logic to NAND only logic.U1,U2 • K4 – Relate AOI logic to NOR only logic.U1,U2 • K5 – Know the rules associated with the K-Mapping Technique.U5,U6	***SKILLS:*** *Students will…* • S1 – Translate a set of design specifications into a functional NAND or NOR combinational logic circuit following a formal design process.U1,U2 • S2 – Compare and contrast the quality of combinational logic designs implemented with AOI, NAND, and NOR logic gates.U2 • S3 – Use Circuit Design Software (CDS) to simulate and prototype NAND and NOR logic circuits. U1 • S4 – Use the K-Mapping technique to simplify combinational logic problems containing two, three, and four variables.U5 • S5 – Solve K-Maps that contain one or more don't care conditions.U6 • S6 – Use current technology to convert AOI designs to universal gate designs.U1,U2

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Evidence *(stage 2)*		
Activities (A) Projects (P) Problems(B)	Assessment FOR Learning	Assessment OF Learning
2.2.1.A K-Mapping: Alternative to Boolean Simplification	• Student responses to examples in presentation 2.2.1 K-Mapping: Alternative to Boolean Simplification • Essential Questions	• Successful completion of simplification problems (12) • Conclusion Questions
2.2.2.A Universal Gates: NAND Only Design	• Student responses to examples in presentation 2.2.2 Universal Gates: NAND Only Design • Essential Questions	• Print out of simulated circuits • Conclusion Questions • Demonstration of completed circuit
2.2.3.A Universal Gates: NOR Only Design	• Student responses to examples in presentation 2.2.3.A Universal Gates: NOR Only Design • Essential Questions	• Print out of simulated circuits • Conclusion Questions • Demonstration of completed circuit
2.2.4.A Conversion Tool: Multisim Logic Convertor	• Essential Questions	• Print out of simulated circuits • Conclusion Questions
2.2.5.P Fireplace Control Circuit: K-Mapping and Universal Gates	• Essential Questions	• Print out of simulated circuits • Conclusion Questions • Demonstration of completed circuit

Learning Plan *(stage 3)*	
Activities (A) Projects (P) Problems(B)	Knowledge and Skills
2.2.1.A K-Mapping: Alternative to Boolean Simplification	K5,S4,S5
2.2.2.A Universal Gates: NAND Only Design	K1,K2,K3,K5,S1,S2,S3,S4,S5, S6
2.2.3.A Universal Gates: NOR Only Design	K1,K2,K4,K5,S1,S2,S3,S4,S5, S6
2.2.4.A Conversion Tool: Multisim Logic Convertor	S3,S6
2.2.5.P Fireplace Control Circuit: K-Mapping and Universal Gates	K1,K2,K3,K4,K5,S1,S2,S3,S4, S5,S6

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