Curriculum Framework – Digital Electronics (2015-2016)
Unit 2 Combinational logic – Lesson 2.1 Combinational Logic Circuit Design

Desired Results *(stage 1)*

ESTABLISHED GOALS
It is expected that students will…

- G1 – Demonstrate an ability to identify, formulate, and solve engineering problems.
- G2 – Demonstrate an ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability.
- G3 – Demonstrate an ability to design and conduct experiments, as well as to analyze and interpret data.
- G4 – Demonstrate an ability to apply knowledge of mathematics, science, and engineering.
- G5 – Demonstrate an ability to use the techniques, skills, and

Transfer

TRANSFER: *Students will be able to independently use their learning to …*

- T1 – Translate a set of design specifications into a functional AOI combinational logic circuit following a formal design process.
- T2 – Recognize and apply simplification strategies to create the most efficient AOI combinational logic circuit design.

Meaning

UNDERSTANDINGS: *Students will understand that …*

- U1 – There is a formal design process for translating a set of design specifications into a functional combinational logic circuit.
- U2 – The first step in designing a combinational logic circuit is to translate a set of design specifications into a truth table.
- U3 – A truth table describes the behavior of a combinational logic design by listing all possible input combinations and the desired output for each.
- U4 – Logic expressions can be derived from a given truth table; likewise, a truth table can be constructed from a given logic expression.
- U5 – All logic expressions can be expressed in one of two forms: sum-of-products (SOP) or products of sum (POS).
- U6 – Simplified logic expressions are used to create

ESSENTIAL QUESTIONS: *Students will keep considering …*

- Q1 – How would you use a design process to convert a set of design specifications into a functional combinational logic circuit?
- Q2 – What is the relationship between a combinational logic circuit's truth table, logic expression, and circuit implementation? Can I describe the process of obtaining either of the first two design items given the third?
- Q3 – When you simplify a logic expression using Boolean algebra, how do you know that you have the simplest solution and that the solution is correct?
- Q4 – In terms of circuit implementation, what is the advantage of representing all logic expression in either the SOP or POS form?
- Q5 – Defend the following statement: "All logic expression, regardless of complexity, can be implemented with AND, OR, and INVERTER Gates."

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modern engineering tools necessary for engineering practice. • G6 – Pursue the broad education necessary to understand the impact of engineering solutions in a global, economic, environmental, and societal context. • G7 – Demonstrate an understanding of professional and ethical responsibility. • G8 – Demonstrate an ability to function on multidisciplinary teams. • G9 – Demonstrate an ability to communicate effectively. • G10 – Gain knowledge of contemporary issues. • G11 – Recognize the need for, and develop an ability to engage in life-long learning.	circuits with fewer gates. • U7 – All logic expressions, whether simplified or not, can be implemented using AND, OR, & INVERTER Gates.	
	Acquisition	
	KNOWLEDGE: *Students will …* • K1 – Know the formal design process for designing combinational logic circuits.U1,U2,U3,U4,U5,U6,U7 • K2 – Know the truth tables and logic expressions associated with AND gates, OR gates, and INVERTER gates.U3,U4 • K3 – Know rules and laws of Boolean Algebra including DeMorgan's Theorems.U5,U6 • K4 – Know that a truth table can be interpreted into an algebraic expression representing the output of the circuit.U3,U4 • K5 – Know that a simplified logic expression can produce the same outputs with fewer gates.U6 • K6 – Recognize sum-of-product expressions and product-of-sum expressions.U5	***SKILLS:*** *Students will …* • S1 – Translate design specifications into truth tables.U2 • S2 – Generate un-simplified logic expressions from truth tables.U4 • S3 – Construct truth tables from logic expressions.U4 • S4 – Formulate simplified logic expressions using the rules and laws of Boolean algebra, including DeMorgan's Theorems.U6 • S5 – Analyze AOI (AND/OR/INVERTER) combinational logic circuits to compare their equivalent logic expressions and truth tables.U4 • S6 – Translate a set of design specifications into a functional AOI combinational logic circuit following a formal design process. U1,U2,U3,U4,U5,U6,U7 • S7 – Simulate and prototype AOI logic circuits using Circuit Design Software (CDS) and a Digital Logic Board (DLB).U1,U2,U3,U4,U5,U6,U7 • S8 – Identify the IC number and recognize the related wiring diagram for AOI Logic.U1

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Evidence *(stage 2)*			Learning Plan *(stage 3)*	
Activities (A) Projects (P) Problems(B)	Assessment FOR Learning	Assessment OF Learning	Activities (A) Projects (P) Problems(B)	Knowledge and Skills
2.1.1.A AOI Design: Truth Tables to Logic Expression	• Student responses to examples in presentation 2.1.1 AOI TT to Logic Expressions • Essential Questions	• Successful analysis of truth tables • Conclusion Questions	2.1.1.A AOI Design: Truth Tables to Logic Expression	K1,K2,K4,S1,S2,S6,S7,S8
2.1.2.A AOI Analysis: Circuit to Truth Table to Logic Expression	• Student responses to examples in presentation 2.1.2 AOI Analysis: Circuit to Truth Table to Logic Expression • Essential Questions	• Successful circuit analysis • Conclusion Questions	2.1.2.A AOI Analysis: Circuit to Truth Table to Logic Expression	K1,K2,K4,S1,S2,S5,S8
2.1.3.A AOI Logic Implementation: Design Specifications	• Student responses to examples in presentation 2.1.3 AOI Logic Implementation: Design Specifications • Essential Questions	• Print out of simulated circuits • Conclusion Questions	2.1.3.A AOI Logic Implementation: Design Specifications	K1,K2,K4,S1,S2,S3,S5,S6,S7, S8
2.1.4.A Circuit Simplification: Boolean Algebra	• Student responses to examples in presentation 2.1.4 Circuit Simplification: Boolean Algebra • Essential Questions	• Successful completion of simplification problems (13) • Print out of simulated circuits • Conclusion Questions	2.1.4.A Circuit Simplification: Boolean Algebra	K2,K3,K4,K5,K6,S2,S4,S7,S8
2.1.5.A Circuit Simplification: DeMorgan's Theorems	• Student responses to examples in presentation 2.1.5 Circuit Simplification: DeMorgan's Theorems • Essential Questions	• Successful completion of simplification problems (6) • Print out of simulated circuits • Conclusion Questions	2.1.5.A Circuit Simplification: DeMorgan's Theorems	K2,K3,K4,K5,K6,S2,S4,S7,S8
2.1.6.P Majority Vote Circuit: AOI Logic Design	• Essential Questions	• Print out of simulated circuits • Demonstration of functioning circuit	2.1.6.P Majority Vote Circuit: AOI Logic Design	K1,K2,K3,K4,K5,K6,S1,S2,S3, S4,S5,S6,S7,S8

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